CLAIMS

1. (Currently Amended) A method for determining wire capacitance for a VLSI circuit design, comprising the steps of:

determining hierarchical blocks of a portion of the design;

storing, for a plurality of the blocks, indicia of a most accurate one of a plurality of wire capacitance data sources;

generating a wire capacitance database with an entry for each net, in at least a plurality of the blocks, using information stored in at least one of the wire capacitance data sources;

generating a hierarchical connectivity model for the design using a single type of connectivity data for each of the blocks; wherein said single type of data is selected from either a layout or a schematic diagram; and

using the hierarchical connectivity model and said wire capacitance database to determine a cumulative wire capacitance value for each high level signal name (HLSN) in each of the blocks in a portion of the design to be analyzed.

2. (Original) The method of claim 1, wherein said cumulative wire capacitance value for each said HLSN is determined by summing the wire capacitance for each said net of each said HLSN.

3. (Original) The method of claim 1, wherein said single type of connectivity data is selected from said layout if all of the connectivity data for the portion of the design to be analyzed is available from the layout.

4. (Original) The method of claim 1, wherein the hierarchical connectivity model for the design is generated by using layout connectivity, if said layout is available for a given said block, otherwise, if no said layout is available for said given block, then by using schematic connectivity data.

5. (Original) The method of claim 1, including the additional steps of:

maintaining a data source indicator associated with each said HLSN; wherein said data source indicator indicates the name of the data source used to generate said wire capacitance;

generating an estimated wire capacitance value for each said HLSN in each of the blocks wherein said wire capacitance is not determined entirely from said most accurate source;

if the data source indicator associated with said HLSN in one of said blocks indicates that the cumulative wire capacitance value is determined entirely from said most accurate source, then using said cumulative wire capacitance value as said wire capacitance for said HLSN; otherwise, if the data source indicator associated with said HLSN in one of said blocks indicates that the cumulative wire capacitance value is not determined entirely from said most accurate source, then using the greater of said estimated wire capacitance value and said cumulative wire capacitance value as said wire capacitance for said HLSN.

6. (Original) The method of claim 5, wherein said data source indicator is used to indicate that said wire capacitance for at least one said net in a particular said HLSN is missing from the wire capacitance database.

7. (Original) The method of claim 5, wherein said data source indicator is a bit vector in which each of a plurality of specifics bits indicates a corresponding said wire capacitance data source.

8. (Original) The method of claim 7, wherein one of the bits in the bit vector is used to indicate that the wire capacitance for a specific said HLSN is missing from the wire capacitance database.

9. (Currently Amended) A method for determining wire capacitance for a VLSI circuit design, comprising the steps of:

(a) determining hierarchical blocks of a portion of the design;

(b) storing, for a plurality of the blocks, indicia of the best available one of a plurality of wire capacitance data sources;

(c) generating a wire capacitance database with an entry for each net, in at least a plurality of the blocks, using information stored in at least one of the wire capacitance data sources;

(d) generating a hierarchical connectivity model for the design using a single type of connectivity data for each of the blocks; wherein said single type of data is selected from either a layout or a schematic diagram;

(e) using the hierarchical connectivity model and said wire capacitance database to determine a cumulative wire capacitance for each high level signal name (HLSN) in each of the blocks in a portion of the design to be analyzed, while maintaining a data source indicator associated with each said HLSN; wherein said data source indicator indicates the name of the data source used to generate said wire capacitance, and wherein the cumulative said wire capacitance for each said HLSN is a total capacitance value determined by summing the wire capacitance for each net in each said HLSN;

(f) generating an estimated wire capacitance for each said HLSN in each of the blocks wherein said wire capacitance is not determined entirely from said best available source;

(g) if the data source indicator associated with said HLSN in one of said blocks indicates that the cumulative wire capacitance is determined entirely from said best available source, then using the total capacitance value generated in step (e) as said cumulative wire capacitance; and

(h) if the data source indicator associated with said HLSN in one of said blocks indicates that the cumulative wire capacitance is not determined entirely from said best available source, then using the greater of the values determined in steps (e) and (f) as said cumulative wire capacitance.

10. (Original) The method of claim 9, further comprising the steps of:

generating an estimated wire capacitance for each said net in each of the blocks for which said wire capacitance is missing from the wire capacitance database; and

for each said HLSN in each of said blocks, if the data source indicator associated with said HLSN in one of said blocks indicates that the cumulative wire capacitance is missing from the wire capacitance database, then using the greater of the values determined in steps (e) and (f) as said cumulative wire capacitance.

11. (Original) The method of claim 10, wherein said data source indicator is used to indicate that said wire capacitance for a given said net is missing from the wire capacitance database.

12. (Original) The method of claim 9, wherein said single type of connectivity data is selected from said layout if all of the connectivity data for the portion of the design to be analyzed is available from the layout.

13. (Original) The method of claim 9, wherein said data source indicator is a bit vector in which each of a plurality of specifics bits indicates a corresponding said wire capacitance data source.

14. (Original) The method of claim 13, wherein one of the bits in the bit vector is used to indicate that the wire capacitance for a specific said HLSN is missing from the wire capacitance database.

15. (Original) The method of claim 9, wherein the hierarchical connectivity model for the design is generated by using layout connectivity, if extracted layout data is available for a given said block, otherwise, if no said extracted layout data is available for said given block, then by using schematic connectivity data.

16. (Currently Amended) A system for determining wire capacitance for a VLSI circuit design comprising:

a processor coupled to a memory device and a data storage unit;

a plurality of data sources, coupled to the processor, each of which generate wire capacitance values for each net in a plurality of blocks in the design;

a wire capacitance database, stored in said data storage unit, wherein said wire capacitance values are stored for each net in a plurality of the blocks in a portion of the design;

a data source directory, stored in said data storage unit, wherein a name of a data source associated with each said high level signal name (HLSN) in each of the blocks in the design;

a plurality of data source indicators, accessible by said processor, for storing indicia of the best available one of a plurality of wire capacitance data sources; and

a plurality of cumulative wire capacitance indicators, accessible by said processor, for storing a cumulative said wire capacitance for each HLSN in each of the blocks in said a portion of the design;

wherein said processor determines all hierarchical blocks of said portion of the design, and generates a hierarchical connectivity model for the design using a single type of connectivity data for each of the blocks, wherein said single type of data is selected from either a layout or a schematic diagram;

wherein the hierarchical connectivity model and said wire capacitance database is used to determine a cumulative wire capacitance for each of said HLSNs in each of the blocks in the portion of the design to be analyzed, while maintaining the data source indicator associated with each of said HLSNs; and

wherein, for each of said HLSNs in each of said blocks, if the data source indicator associated with any of said HLSNs indicates that the cumulative wire capacitance is determined entirely from said best available source, then said cumulative wire capacitance is used as said wire capacitance for each said HLSN in each of said blocks; otherwise, the greater of an estimated wire capacitance and said cumulative wire

capacitance is used as said wire capacitance for each of said HLSNs in each of said blocks.

17. (Original) The system of claim 16, wherein the cumulative said wire capacitance for each of said HLSNs is determined by summing the wire capacitance for each of the nets in each of said HLSNs.

18. (Original) The system of claim 16, wherein:

an estimated wire capacitance is generated for each said net in each of the blocks for which said wire capacitance is missing from the wire capacitance database; and

for each of said HLSNs in each of said blocks, if the data source indicator associated with one of said HLSNs in one of said blocks indicates that the cumulative wire capacitance is missing from the wire capacitance database, then using the greater of said estimated wire capacitance and said cumulative wire capacitance is used as said wire capacitance for each corresponding one of said HLSNs in each of said blocks.

19. (Currently Amended) A system for determining wire capacitance for a VLSI circuit design, comprising:

means for determining all hierarchical blocks of a portion of the design;

means for storing, for a plurality of the blocks, indicia of the best available one of a plurality of wire capacitance data sources;

means for generating a wire capacitance database with an entry for each net in at least a plurality of the blocks, using information stored in at least one of the wire capacitance data sources;

means for generating a hierarchical connectivity model for the design using a single type of connectivity data for each of the blocks; wherein said single type of data is selected from either a layout or a schematic diagram; and

means for calculating a cumulative wire capacitance value for each high level signal name (HLSN) in each of the blocks in a portion of the design to

be analyzed, using the hierarchical connectivity model and said wire capacitance database.

20. (Currently Amended) A software product comprising instructions, stored on computer-readable media, wherein the instructions, when executed by a computer, perform steps for determining wire capacitance for a VLSI circuit design, comprising:

instructions for determining all hierarchical blocks of a portion of the design;

storing, for a plurality of the blocks, indicia of the best available one of a plurality of wire capacitance data sources;

instructions for generating a wire capacitance database with an entry for each net in at least a plurality of the blocks, using information stored in at least one of the wire capacitance data sources;

instructions for generating a hierarchical connectivity model for the design using a single type of connectivity data for each of the blocks; wherein said single type of data is selected from either a layout or a schematic diagram; and

instructions for using the hierarchical connectivity model and said wire capacitance database to determine a cumulative wire capacitance value for each high level signal name~~HLSN~~ in each of the blocks in a portion of the design to be analyzed.

21. (Currently Amended) A system for determining wire capacitance for a VLSI circuit design, comprising:

means for determining all hierarchical blocks of a portion of the design;

means for storing, for a plurality of the blocks, indicia of the most accurate one of a plurality of wire capacitance data sources;

means for generating a wire capacitance database with an entry for each net in at least a plurality of the blocks, using information stored in at least one of the wire capacitance data sources; and

means for generating a hierarchical connectivity model for the design using a single type of connectivity data for each of the blocks; wherein said

single type of data is selected from either layout or a schematic diagram;

wherein the hierarchical connectivity model and said wire capacitance database is used to determine a cumulative wire capacitance value for each high level signal name~~HLSN~~ in each of the blocks in a portion of the design to be analyzed.